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(12) United States Patent
Tanada

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(54) CIRCUIT FOR INSPECTING SEMICONDUCTOR DEVICE AND INSPECTING METHOD

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(73) Assignee: Semiconductor Energy Laboratory Co., Ltd. (JP)

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See application file for complete search history.

(56) References Cited

U.S. PATENT DOCUMENTS

4,775,891 A * 10/1988 Aoki et al. 348/572
5,068,547 A * 11/1991 Gascoyne 326/16
5,410,247 A * 4/1995 Ishizuka 324/158.1
5,825,204 A * 10/1998 Hashimoto 326/54
6,455,336 B1 * 9/2002 Berndlmaier et al. 438/14
6,573,774 B1 * 6/2003 Gardner 327/201
6,711,041 B2 * 3/2004 Pereira et al. 365/49
6,762,617 B2 * 7/2004 Iwase et al. 326/11
6,762,735 B2 7/2004 Koyama 345/76
6,850,080 B2 2/2005 Hiroki 324/750
2001/0035526 A1 11/2001 Yamazaki et al. 257/57
2001/0040565 A1 11/2001 Koyama 345/204
2002/0130675 A1 9/2002 Hiroki 324/750
2002/0132383 A1 9/2002 Hiroki et al. 438/17
2004/0119824 A1 6/2004 Osada 348/180

(Continued)

FOREIGN PATENT DOCUMENTS

JP 05-256914 10/1993

(Continued)

OTHER PUBLICATIONS

International Search Report for application No. PCT/JP2004/003549, dated Apr. 27, 2004 (In Japanese).

(Continued)

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(57) ABSTRACT

It is configured by plurality of NAND circuits connected in series through a plurality of inverters, and a plurality of NOR circuits connected in series through the plurality of inverters. Each of a plurality of source signal lines provided in a pixel portion is connected to one input terminal of a NAND circuit and a NOR circuit, and an output of an inspection is obtained from final lines of the NAND circuit and the NOR circuit connected in series. In this manner, an inspecting circuit which is capable of determining a defect simply and accurately by using a small-scale circuit, and a method thereof are provided.

25 Claims, 17 Drawing Sheets